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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/017,073

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Nagabhushana T. Sindhushayana

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08/23/2005

Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER

PERILLA, JASON M

ART UNIT

PAPER NUMBER

2638

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/017,073

Applicant(s)

SINDHUSHAYANA ET AL.

Examiner

Jason M. Perilla

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 8, 9, 13 and 25-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 25, 26 and 31-34 is/are rejected.
- 7) ☒ Claim(s) 1-3, 8, 9, 13 and 27-30 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 June 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-3, 8, 9, 13, and 25-34 are pending in the instant application.

Response to Arguments/Amendments

2. In view of the amendments to the claims and the Applicant's remarks filed June 8, 2005, the prior art rejections set forth in the first office action dated March 10, 2005 have been withdrawn.
3. New rejections are set forth below.

Claim Objections

4. Claims 1-3, 8, 9, 13, and 25-34 are objected to because of the following informalities:

Regarding claim 1, the claim is objected to because, according to the claim, the programmable rotator takes as input both a function of the phase increment signal and an accumulation of the phase error of the received signal. However, according to figure 1, such claimed subject matter is not shown. That is, the phase rotator 126 takes only one control as input. Likewise, the rotator 130 takes only one control as input. The following amendment to the claim is presented by the Examiner to overcome the objection:

1. A searcher for finding the frequency of a received signal comprising a phase error, the searcher comprising:
 - a frequency locked loop that generates a phase increment signal in response to the phase error of the received signal;
 - a programmable rotator coupled to the frequency locked loop, the programmable rotator performing a phase rotation function ~~in response to the phase increment signal~~;
 - a phase error accumulator accumulating ~~results of the phase error increment~~ signals from the frequency locked loop and generating a control signal that instructs the programmable rotator to perform the phase rotation function; and
 - a shift register coupled between the phase error accumulator and the programmable rotator, the shift register truncating a predetermined number of bits of the control signal.

Regarding claim 25, the claim is objected to because it does not properly embody the invention. That is, it limits the invention to that which is outside the scope of the invention according to the specification and drawings. The claim provides for a first and second phase rotator each configured to phase rotate a signal. However, according to the illustration of the invention according to figure 1, the first rotator (126) rotates the signal (112) and the second rotator (130) rotates that which is output from the first rotator. According to the claim, each of the rotators acts upon the signal (112) directly. In figure 1 of the drawings, it would not be appropriate to label both the input and the output of the first rotator (126) with the same reference (i.e. the same signal).

Regarding claim 31, the claim is objected to for the same reasons as applied to claim 25 above regarding the first and second instances of phase rotating a signal.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 31-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 31, the claim is indefinite because the first (line 3) and second (line 7) instances of phase rotating are not distinguished in the claim. One is unable to determine if both the instances are to be interpreted as one step or more than one step.

Further, the order of the first and second phase rotating with respect to the remaining steps in the method may not be definitively determined.

Regarding claim 32, the claim is rejected as being based upon a rejected parent claim.

Regarding claim 33, one is unable to determine if the further limitation to "the phase rotating" is applied to the first or second instance of phase rotating in the parent claim.

Regarding claim 34, one is unable to determine if the further limitation to "the phase rotating" is applied to the first or second instance of phase rotating in the parent claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 25, 26, 31 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Asahara et al (US 6631174; hereafter "Asahara").

Regarding claim 25, Asahara discloses according to figure 18 a searcher for finding the frequency of a received signal (title; abstract) comprising a plurality of segments, the searcher comprising: a first phase rotator (10a) configured to phase

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rotate a signal (I/F SIGNAL) to partially reduce a phase error (col. 32, lines 12-27) of the signal and produce a first phase rotator output signal; an accumulator (9b) configured to accumulate a plurality of chips to form segments from the first phase rotator output signal; a second rotator (10b) configured to phase rotate the signal to further reduce the phase error of the signal by adjusting the phase over each segment (col. 32, lines 40-45). The received signal (I/F SIGNAL) of Asahara, as broadly as claimed, is considered to contain a plurality of segments which are phase rotated and accumulated. The first phase rotator output signal, according to Asahara, is fed into a frequency deviation estimating section (8; col. 32, lines 25-33) to detect the remaining frequency deviation after the first phase rotator is applied. This remaining frequency deviation may be integrated or accumulated in integrators 9a or 9b (col. 32, lines 39-45) to be subsequently applied to either of the corresponding phase rotators 10a or 10b. As broadly as claimed, a segment of the first phase rotator output signal is accumulated and output by the 9b. The input to the integrator 9b can be considered to be "chips" of frequency error remaining in the received signal after the first phase rotator is applied.

Regarding claim 26, Asahara discloses the limitations of claim 25 as applied above. Further, Asahara discloses that the second rotator (fig. 18, ref. 10b) is implemented within a frequency locked loop (title; fig. 18), the frequency locked loop producing a phase increment signal (input to integrator 9a) based on the phase error, the first phase rotator (10a) configured to phase rotate the signal (I/F SIGNAL) based on an accumulation of the phase increment signal (col. 32, lines 13-18).

Regarding claims 31 and 32, the claims are disclosed by Asahara as applied to claims 25 and 26, respectively, above.

Allowable Subject Matter

9. The indication of allowable subject matter is made regarding claims 1-3, 8, 9, 13.

10. The following is a statement of reasons for the indication of allowable subject matter:

Claims 1-3, 8, 9, 13 are indicated to contain allowable subject matter because the prior art of record does not disclose the claimed subject matter. That is, the prior art of record does not disclose a frequency locked loop wherein a control signal generated by an accumulator and applied to a phase rotator is truncated by a predetermined number of bits using a shift register before it is applied to the phase rotator. Further, the prior art of record does not provide, collectively, the proper motivation to utilize such a shift register between an accumulator and a phase rotator in a frequency locked loop. While the prior art of record discloses a frequency locked loop having an accumulator which provides a control signal to a rotator and, separately, shift registers utilized for truncating bits, one skilled in the art may not be motivated to utilize a prior art truncating shift register in a prior art frequency locked loop because, among other reasons, the two prior art inventions may be incompatible. The use of a truncating shift register in a common prior art frequency locked loop must provide an advantage. However, in the prior art of record, no proper advantage for the combination is identified.

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11. Claims 27-30, 33 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following claims 25 and 31, drafted by the examiner and considered to distinguish patentably over the art of record in this application, are presented to applicant for consideration:

25. A searcher for finding the frequency of a received signal comprising a plurality of segments, the searcher comprising:
a first phase rotator configured to phase rotate a signal to partially reduce a phase error of the signal and produce a first phase rotator output signal;
an accumulator configured to accumulate a plurality of chips from the first phase rotator output signal to form segments ~~from~~ of the first phase rotator output signal; and
a second rotator configured to phase rotate the segments of the first phase rotator output signal to further reduce the phase error of the signal by adjusting the phase over each segment; and
wherein the second rotator is implemented within a frequency locked loop producing a phase increment signal based on the phase error, the first phase rotator configured to phase rotate the signal based on an accumulation of the phase increment signal.

31. A method of finding a signal having a deviation from an expected frequency, the method comprising:
first phase rotating a signal to partially reduce a phase error of the signal and produce a partially rotated output signal;
accumulating a plurality of chips from the partially rotated output signal to form segments ~~from~~ of the partially rotated output signal; and
second phase rotating the segments of the partially rotated output signal to further reduce the phase error of the signal by adjusting the phase over each segment; and
generating a phase increment signal based on the phase error, the first phase rotating the signal to partially reduce the phase error based on an accumulation of the phase increment signal.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to

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further show the state of the art with respect to frequency locked loops and truncating shift registers.

U.S. Pat. No. 4769826 to Kubo et al.

U.S. Pat. No. 4943982 to O'Neil et al.

U.S. Pat. No. 5440587 to Ishikawa et al.

U.S. Pat. No. 5471508 to Koslov.

U.S. Pat. No. 6363102 to Ling.

U.S. Pat. No. 6393083 to Beukema.

U.S. Pat. No. 6570946 to Hormol et al.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
August 22, 2005

jmp


CHIEH M. FAN
PRIMARY EXAMINER